REMARKS

Claims 1, 2, and 4-30 are pending in the application. Claims 1-18 and 20-25 stand rejected as allegedly being anticipated by U.S. Patent No. 5,898,866 to Atkins et al. ("Atkins"). Claims 26-30 stand rejected as allegedly being obvious in view of Atkins. Claim 19 stands rejected as allegedly being obvious over Atkins in view of U.S. Patent No. 6,003,128 to Tran ("Tran").

In view of the remarks herein, the rejections are respectfully traversed.

Claim 1

Claim 1 is patentable over Atkins at least because Atkins neither teaches nor suggests "defining, within a computer program, loop conditions corresponding to a particular instance of a loop setup instruction for a first hardware loop," as recited in claim 1.

The office action states that "Atkins has several pipelines, where several different loops can be executed in parallel with each other, since more than one SETLOOP instruction could be present and each one can be present in a different pipeline; also the situation would exist where the two pipelines are executing different instances of the same instruction group, or same SETLOOP instruction, thereby being

the same hardware loop..." (Please see paragraph 3 of the office action. That is, although the office action does not identify any particular teaching that loop conditions of a hardware loop are propagated in parallel via first and second pipelines of a pipelined processor (as outlined in the previous version of claim 1), the office action bases its rejection on speculation that the system of Atkins can do so.

However, this is not sufficient to present a prima facie case of anticipation. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Please see MPEP 2131.01). Further, "The elements must be arranged as required by the claim..." (Please see MPEP 2131.01). A speculation that the elements of the claim can be present in a system described by a particular reference teachings is neither a direct nor an inherent description of the claim elements.

However, claim 1 has been amended to further emphasize patentable aspects. Claim 1 has been amended to include the features that the loop conditions correspond to a particular instance of a loop setup instruction, to address the office action's concern that the system of Atkins can have more than one SETLOOP instruction present in different pipelines.

It is respectfully noted that Atkins neither teaches nor suggests this feature of claim 1. For at least this reason, claim 1 is patentable over Atkins.

Claims 2-6

Claims 2-6 depend from claim 1, and are thus patentable for at least the same reasons as noted above with respect to claim 1.

Claim 2

Claim 2 is patentable for at least the additional reason that Atkins neither teaches nor suggests writing loop conditions to first and second sets of registers, "wherein the second different set of registers comprises one or more architectural pipeline registers," as recited in claim 2.

The office action notes that Atkins teaches a pipelined processor. In a pipelined processor, a loop setup instruction would normally be committed to an architectural register after exiting the write back stage. (Please see page 7, lines 12-14 of the current specification). However, because the loop entry and exit conditions stored in an architectural register may not be updated until several cycles have passed from when the loop setup instruction entered the pipeline, there may be delays on setting up hardware loops. (Please see page 7, lines 14-20 of the current specification). Using a separate first set of registers (e.g., a set of early registers as described on page 8

line 3 et seq. of the current specification) may increase processing speed by reducing or avoiding loop set up penalties. (Please see page 8, lines 8-10 of the current specification).

For at least the additional reason that Atkins neither teaches nor suggests this feature of claim 2, claim 2 is patentable over Atkins.

Claim 7-12

Claim 7 includes features similar to those discussed above with respect to claim 1, and is therefore patentable for at least similar reasons. Claims 8-12 depend from claim 7, and are therefore patentable for at least the same reasons.

Claims 13-21

Claim 13 includes features similar to those discussed above with respect to claim 1, and is therefore patentable for at least similar reasons. Claims 14-21 depend from claim 13, and are therefore patentable for at least the same reasons.

Claims 22-27

Claim 22 includes features similar to those discussed above with respect to claim 1, and is therefore patentable for at least similar reasons. Claims 23-27 depend from claim 22, and are therefore patentable for at least the same reasons.

Claim 28

Claim 28 stands rejected under 35 U.S.C. 103 as allegedly being unpatentable over Atkins. However, claim 28 is patentable

over Atkins because Atkins neither teaches nor suggests a processor adapted to "propagate at least one of the loop conditions of said first hardware loop to the second set of registers via the first pipeline;" "propagate at least one of the loop conditions of said first hardware loop to the second set of registers via the second pipeline," and a control unit of the processor adapted to "begin calculating data using said first hardware loop prior to completing said first and second propagate," as recited in claim 28.

Claim 28 recites a system adapted to calculate data using a hardware loop, but in a special way. Loop conditions are propagated to a set of registers via first and second pipelines. Additionally, before the propagating acts are completed, data calculation using the first hardware loop is begun.

Atkins neither teaches nor suggests such a system. The office action alleges that Atkins teaches the propagate acts because "the situation would exist where the two pipelines are executing different instances of the same instruction group, or same SETLOOP instruction, thereby being the same hardware loop." (Please see paragraph 32 of the office action). Even if this speculation were correct, Atkins would need to further teach that, prior to the two pipelines completing execution of the different instances of the same instruction group, the hardware loop would begin calculating data.

Atkins does not so teach. In fact, if two separate pipelines were executing different instances of the same instruction group for the first hardware loop contemporaneously (so that the "begin calculating data..." act would be done prior to completing the first and second propagate acts), a conflict would arise. Both pipelines would be using the same hardware loop to implement different instances of the loop instructions.

The office action alleges that Atkins teaches the "begin calculating data..." feature of claim 28 because "the counts are decremented before the new values are propagated to determine if the process is at the end of the loop," and that "the 'propagating' is not clearly defined and can be broadly interpreted to mean propagating any of conditions at any time in the process." (Please see paragraph 32 of the office action).

However, it is respectfully noted that cited teaching refers to a single instance of a loop execution. Therefore, the cited portion of Atkins cannot be said to teach that the "begin calculating ..." act is performed prior to completing both the first and second propagating acts (which, according to the office action, are related to separate instances of loop execution).

At least because Atkins neither teaches nor suggests the above features of claim 28, claim 28 is patentable over Atkins.

Claims 29-30

Claims 29-30 depend from claim 28, and are therefore patentable for at least the same reasons as outlined above with respect to claim 28.

CONCLUSION

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue, or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Claims 1, 2, and 4-30 are in condition for allowance, and a notice to that effect is respectfully solicited. If the Examiner has any questions regarding this response, the Examiner is invited to telephone the undersigned at (858) 678-4311.

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No fees are believed due. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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